ORIGINAL

Insulating Biomaterials
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1/30/98

Introduction

Work on the large scale instrumentation for monitoring many devices at 37°C, 60°C, and 90°C has been completed for the 90°C system and is now being extended to the 37°C system. New devices using University of Michigan technology are being prepared for in-vitro and in-vivo testing encapsulated with silicones. Microstimulators from Mehmet Dokmeci of Dr. Najafi's group at the University of Michigan were received and are being encapsulated with silicones to hopefully prevent the corrosion of the polysilicon traces previously observed. Mr. Dokmeci prepared a set of all tantalum-iridium substrates for our use in testing silicones since their normal metallization system did not survive our cleaning sequence. The devices were visually inspected and were excellent. We are now preparing the devices for bonding, encapsulation and testing using the two interdigitated finger arrays that they use for dew point sensing. This will allow direct testing of our encapsulation techniques on UM substrates. The focus of the remainder of this report is on development of the Passivation Chip (Pass Chip) that will be used to further understand long term failure modes for implantable MOS integrated circuits. This structure is the result of several years of work to develop a long term test vehicle for monitoring the degradation of various components of implantable microelectronics in the central nervous system of animals.

Passivation Chip for MOS Devices

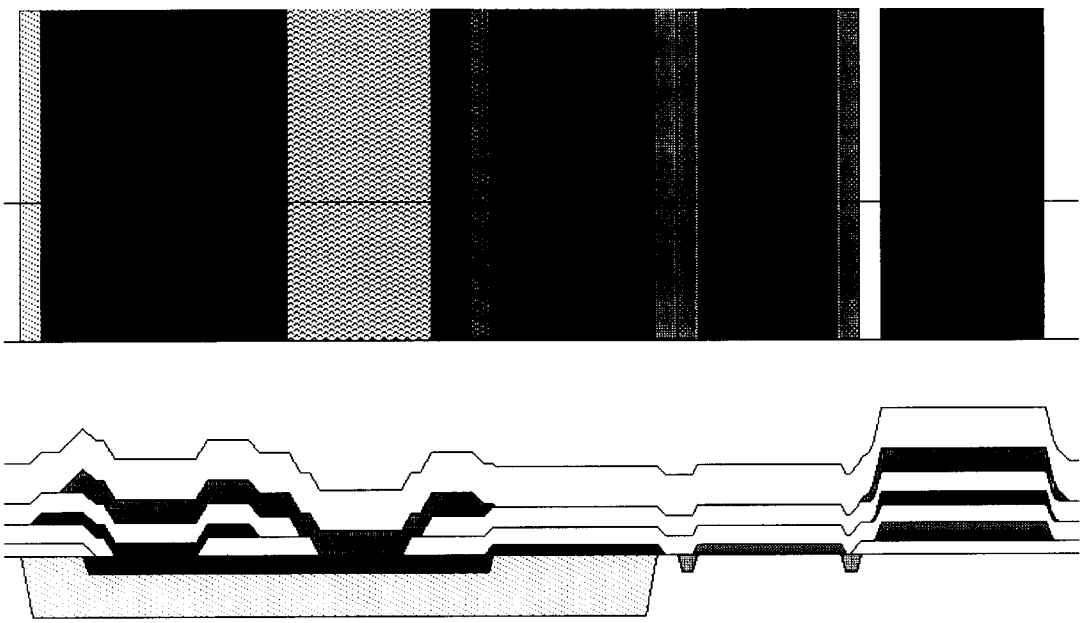

Figure 1: Examples of the many conductors and dielectrics used in typical CMOS integrated circuits. This example is from the MOSIS n-well 2μm process.

The PassChip designed this quarter was developed to allow *in-vivo* testing of basic elements of integrated circuits. In the past, simple silicon devices with interdigitated

electrode arrays were fabricated and were used to evaluate surface encapsulants. While these devices have yielded important information concerning appropriate encapsulants for passive silicon devices, silicon integrated circuits have more possible failure modes than failure of the surface encapsulation. For example, as shown in Figure 1, silicon integrated circuits typically use a variety of dielectric layers. Some of these layers contain soluble materials such as boron and/or phosphorous that could lead to formation of low conductivity pathways and corrosion. MOS devices require low leakage, charge stable dielectrics for many circuit applications. Intrusion of water and ions from the biological environment can cause increased electrical leakage through gate oxides and could also alter the fixed charge within the oxide. There are perhaps other long term failure modes as well that have yet to be discovered since there is little experience with embedding MOS integrated circuits within biological systems unless they are within hermetically sealed titanium canisters as in pacemaker applications.

Oxide monitors were developed in previous work to monitor slow leakage of electrons off of MOS gate capacitors. The devices worked by providing charge to a perforated MOS gate through an ultraviolet (UV) light programmable capacitor. While this is a very sensitive measurement, transients that can occur during handling made it difficult to maintain long term testing. Once discharged, the devices could not be re-charged because of the encapsulation blocked the UV required for programming.

In order to better test various components and elements of MOS integrated circuits, the PassChip was designed to evaluate intra-level leakage currents as well as inter-level leakage currents through the various dielectric layers, all of which are important for operation of circuits. The threshold voltages for Schmitt trigger voltage sensors were monitored by the channel marker interval which was inversely proportional to the Schmitt trigger threshold. Reversed biased diodes protected by metal 2 and unprotected monitor PN junction leakage currents for detection of water and ionic contamination of the silicon substrate. Test devices for monitoring the surface leakage currents of metal traces encapsulated with silicones or other appropriate materials were included. Bond pads for monitoring an external device allow for testing of wire insulation as one example.

To make all of these tests possible, it was necessary to identify or develop a power supply that could provide a stable voltage for the lifetime of the implant. Since the devices were to be implanted in animals, it was desirable to find a power supply that could be implanted as well to avoid the need for percutaneous conduits and wearable vests with wired interconnects. The miniature battery packs used to bias the subcutaneous hip implants for the past several years could not supply the required power necessary for continuous operation of the circuit. While various schemes were devised for switching devices on and off to conserve battery power, the miniature packs were still too tall if located on the head. **Figure 2** shows a cartoon of what the miniature battery packs look like when installed on a 12 pin percutaneous connector. For long term implants, the high aspect ratio of even the miniature battery packs severely jeopardizes the integrity of the implant, especially when the animals bump against the cage when startled or even when feeding from standard troughs.

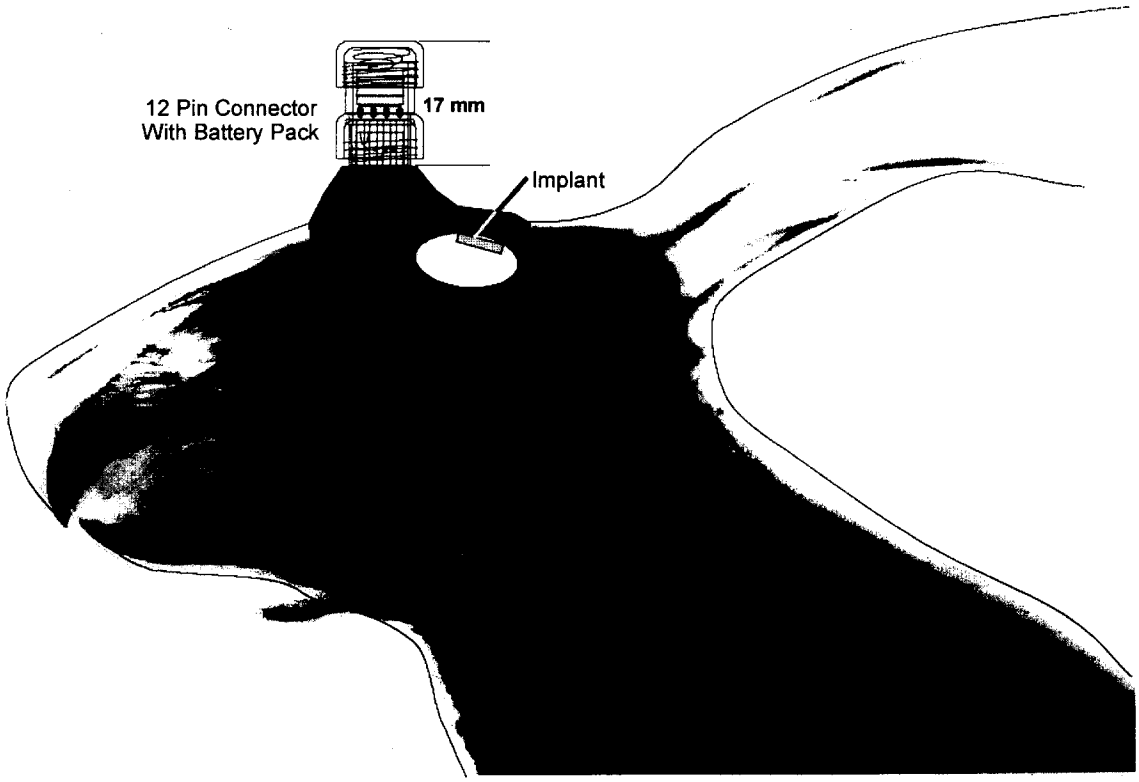

Figure 2: Cartoon of subdural implant with percutaneous pedestal, 12 pin connector and miniature battery pack.

Implantable solar panels were also investigated as a continuous source of power. We have used such panels in other implantable applications for over one year with good results, but there was no requirement in those applications for continuous power.

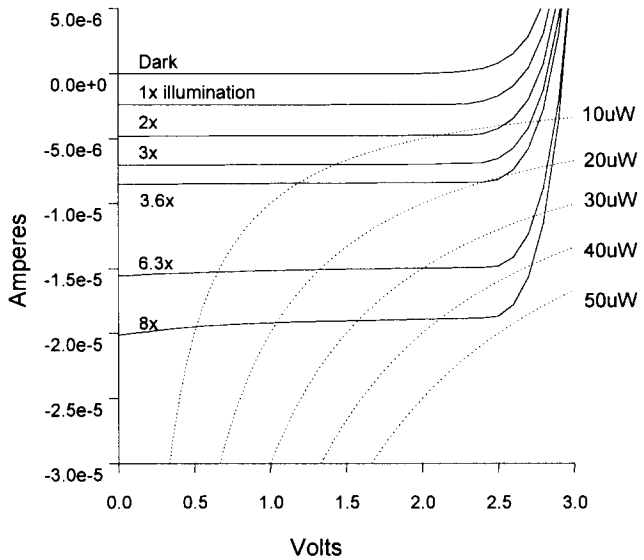

Figure 3: IV plots of 6 element solar panel 2x2mm square. 1x illumination was approximately equivalent to bright room light.

Figure 3 shows results of a 6 element solar panel (2x2mm square total) illuminated with various light intensities from bright room light (1x) and up. Two of these panels could power a limited bandwidth, low power implanted circuit. However, since animals move around and there are many shadows in normal rabbit cages, it would be difficult to reliably illuminate implanted power panels even with strong infrared sources. Thus some means of turning off the active circuitry while maintaining the required 5 volt bias was needed. Again, various schemes were developed and evaluated. While this approach could possibly work, there was considerable overhead to the maintenance of constant illumination in an animal facility, even at modest levels. Also, whether or not there was constant illumination would always be questionable.

In parallel with the above efforts to develop a viable plan for long term biasing and operation of an implanted PassChip, we investigated a number of different battery technologies such as silver oxide, nickel cadmium, and various types of lithium. Most technologies were too large for subcutaneous implantation on the rabbit head or neck, or could not provide sufficient power for long term circuit operation. Another fault of most available battery technologies was the tendency for the seal between the anode and cathode to fail during long term immersion in saline even though encapsulated with silicones of various types. Part of the issue was the cleaning procedure used prior to encapsulation which could not be aggressive. Eventually we came across a new lithium battery technology manufactured by Tadiran Corporation. These batteries use a lithium thionyl chloride chemistry. The batteries are hermetically sealed with a special sealing glass that can withstand the corrosive properties of the lithium chemistry. Since there are no vents, and the anode-cathode seal/spacer was some type of glass, it seemed reasonably likely that silicone encapsulation could work. A typical low level discharge curve for the Tadiran type 2186 lithium battery is shown in Figure 4. While the discharge current is only 4μAmperes, the voltage remains stable at 3.5 volts for over 9 years.

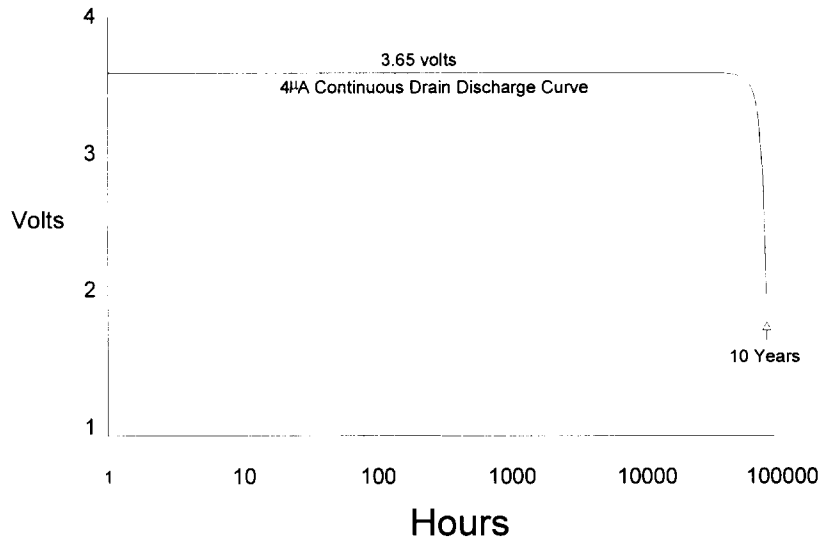

Figure 4: Tadiran, Inc. Lithium-Thionyl Chloride battery type 2186 discharge curve illustrating stability at 3.65 volts for over 9 years.

In view of recent work we have accomplished on low noise/power circuit design techniques, it appeared possible to develop a circuit that could operate at less than 4μA of current. However, the possibility of encapsulating the Tadiran lithium battery technology had to be demonstrated. Accordingly, two Tadiran-2186 glass sealed lithium-thionyl chloride batteries were encapsulated with Nusil CF20-2186 silicone encapsulant. The batteries survived curing of the silicone at 50°C and were then placed under 37°C saline soak. Periodically, the battery voltage was measured. For over one year so far the voltage has not degraded measurably. While the residual power in these batteries is not known, it is likely that if there was significant leakage between the anode and cathode along the glass seal under the silicone, there would be traces of corrosion. Thus far, no traces of corrosion on the glass seal or any other part of the encapsulated batteries have been observed.

One major issue with an automated test system that could be implanted was how to best transduce the low level currents being measured into a useable readout. In-vitro testing utilizes expensive, large, high value resistors in current to voltage converting electrometers to provide sensitive readout of low level signals. However, since IC dielectrics are very good insulators, it may be that the leakage currents would be difficult to sense even with very high value resistors.

An alternative was to use a charge integrator with low leakage MOS integration capacitors. One issue with charge integrators is that the charge on the integration capacitors must be periodically reset. The leakage currents imposed by the reset connection to the integration node limits the ultimate sensitivity of the system. While we did not have reliable measurements of MOS diode leakage currents, they were estimated to be between 1-10 x 10^{-17}amperes/μm^2. Thus with a minimum size geometry drain diffusion (42μm^2), in a well biased at the potential of the integration node, parasitic leakage current should be less than 42-420x10^{-17}amperes which should be sufficient for this work.

An ultra-low power method for reading out the information would be to simply generate a pulse during the resetting of a charge integrator. The time between pulses would then be inversely proportional to the leakage current onto the integration capacitor. This pulse position modulation scheme was successfully used in other applications and does indeed result in very low average power consumption for transmission of data. Further, it is a low noise system because the data is encoded in the interval between pulses and is relatively independent of pulse amplitude. However, very low leakage current test structures would be very difficult to detect since the pulses could occur with very long inter-pulse intervals. Thus, a channel that was not functioning could look like a channel that simply had very low leakage currents. Setting minimum intervals for each channel reduces the overall sensitivity of the system. In addition to these considerations, some means of detecting open circuited sensors was needed to avoid confusing open circuits with low leakage currents.

Figure 5 is a sketch of a system that allows independent integration of leakage currents from multiple sources, multiplexing of the information, pulse position encoding of the data, and transmission of the signals. The system is designed to work as follows.

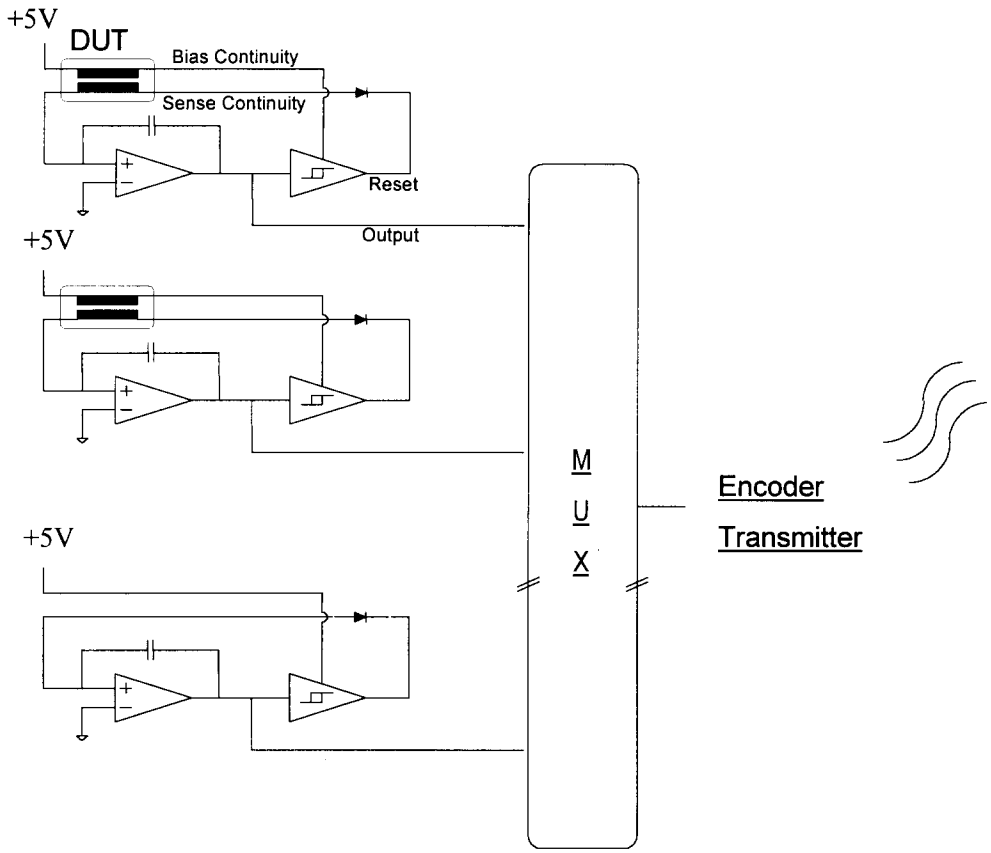

Figure 5: Sketch of charge integrator, multiplexed leakage current monitor concept. Note there is one encoder/transmitter for an arbitrary number of channels.

Under 5 volt bias, the leakage currents through a Device Under Test (DUT) flow onto a small integration capacitor in the feedback loop of an operational amplifier. The output of the amplifier falls as charge accumulates on the integration capacitor. When the output of the integration capacitor crosses the threshold of a Schmitt Trigger detector, the integration node is reset through a low leakage current diode in effect. The actual data output of the charge integrator is the voltage level of the integrator which is proportional to the total charge on the integration capacitor. By reading out this voltage at a rate faster than the reset rate of the integrator, multiple samples of the integration output can be obtained before the integrator is reset. The derivative of the integrator output with respect to time is proportional to the leakage current. During a given measurement episode where the readout of the devices are recorded, if there is no detectable change in the output from a particular integrator, then that device may need to be monitored at daily or longer intervals to detect the leakage current. Thus the dynamic range of the system can be quite high. For example, with the readout rate set at 100Hz for the 14 channel (including marker) device recently designed, each channel would be readout every 0.14 seconds. Thus if the fastest integrator reset occurred every 1 second, multiple samples of the integration slope could still be obtained. By designing the integration capacitor to be 2pF, the highest leakage current that could be easily monitored would be 5V x 2pF / 1sec = 10^{-11}amperes. Higher leakage currents

would begin to exhibit aliasing since the sample rate would be too low. However, for the devices being considered here, leakage currents higher than 10^{-12}amperes would indicate significant device degradation. The lowest current that can be monitored with this design is limited by the parasitic leakages associated with the integration node, probably dominated by the reset switch (~40-400x10^{-17}amperes). A 4x10^{-16}ampere leakage current would take approximately 50 seconds to cause a 10mV shift in the output of the integrator. The noise level of the system is expected to be much less than 10mV, so this signal should be easily detected. By monitoring for a few minutes then, it should be possible to gather enough data to accurately measure the integration slope. While the leakage current associated with the reset switch could be minimized further by various guard techniques, it is useful to have a positive leakage current that will show that the integrator is functioning normally in the absence of leakage current from the DUT. By including an integrator that simply measures it's own leakage current, the actual parasitic leakage currents can be documented.

It was also important to include in the circuit architecture a means of detecting whether or not the interconnects to the device under test were indeed connected. If either interconnect failed, the device could be open circuited and could thus output erroneous very low leakage current readings. To detect this condition, the bias voltage connection to the device under test was used also as the power supply connection for the integrator/detector stage as shown in Figure 5. Also, the sensing connection to the integration node was also used as the reset interconnect. If either failed, the integrator output would fall to ground and would remain stable over time. This is an odd condition for the system because it implies that there is a very high input current to the integrator, but the integrator output does not change. Thus it is a unique fault condition that cannot be confused with a low leakage current condition. Channel marking was accomplished by sending the power supply voltage to the output stage. Since the individual integrators only reset the integrator output to the Schmitt Trigger threshold, the power supply output voltage is also unique and can be used to detect channel 1 for de-multiplexing the transmitted signal.

Using principals of low noise/low power circuit design techniques developed during a Master's thesis [Larson, 1996 #62], sufficiently low noise and low power circuit modules were designed to allow operation of a PassChip with up to 21 sensors on less than 4μA of power. In order to provide approximately 5 volts of bias across test devices, two lithium batteries would be used. Also from prior work, we had considerable experience with ultra-low power transcutaneous transmission of relatively low bandwidth data using pulse position modulated pulses of light. By using short pulses and relatively long intervals, it was possible to keep the designed average current draw on the batteries to less than 4μA. In previous work we developed an LED transmitter that used pulse position modulated light pulses for transcutaneous transmission. For over 2 years we have had LEDs and encapsulated circuitry under saline soak with good results. The overall implant scheme is shown in Figure 6. The lithium batteries should last for over 9 years. If the battery potential falls, the channel marker interval will also fall. In the absence of other indicators of circuit degradation, this would indicate failure of the power supply. Under these conditions, it would be possible to replace the batteries in a

short, minimally invasive surgery, though this should not be necessary. Lead breakage may occur between the batteries and the implant, but hopefully by using relatively large, multistrand, Teflon® insulated wires that are twisted together into a helix, the probability of this happening will be minimized.

Readout of the implants will require minimal restraint of the animal for up to 10 minutes which will greatly facilitate routine data collection from the implanted devices. A hand held photodetector will convert the LED outputs to a pulse train which will be de-multiplexed and decoded using analog circuitry. The reconstructed signals will then be acquired by a data acquisition computer and the leakage currents computed and archived.

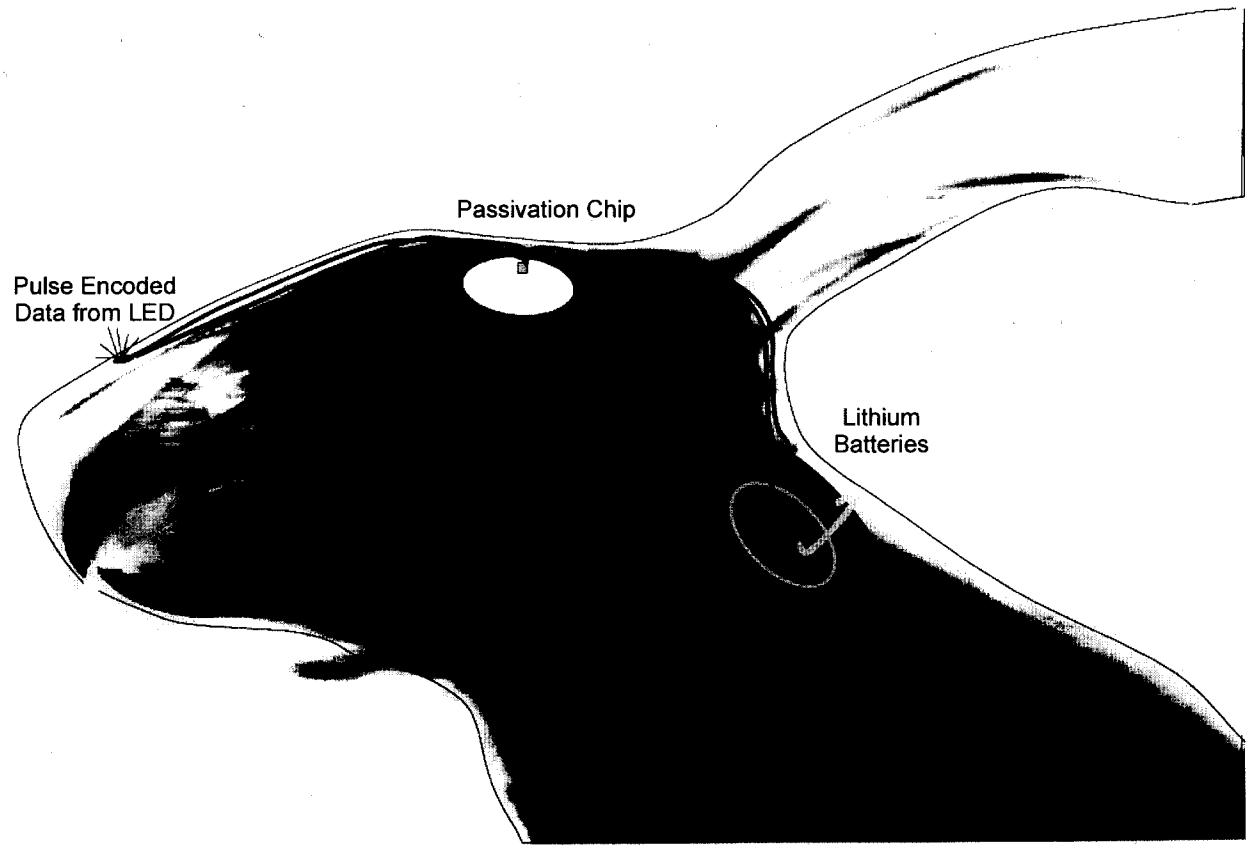

Figure 6: Sketch overlayed on x-ray of rabbit showing planned locations for components of totally implanted PassChip sensor telemetry system.

A test circuit for these concepts shown in Figure 7 was designed and submitted to MOSIS for fabrication in November. This test circuit was our first attempt at bringing together a number of design concepts. There were 5 circuit related bond pads for connecting an external bias setting resistor, power supply, the LED output, and the photodiode reset for initializing the shift register after power up. There is an on-chip photodiode for the same purpose, but in the event that it is necessary to reset the system after implantation – perhaps after a battery change, the external connection could be used. The V+/shield connection was originally included to allow connection of

the Metal 2 shield to either power or ground or to leave it floating. However, in this particular layout an error caused the shield to be connected to V+.

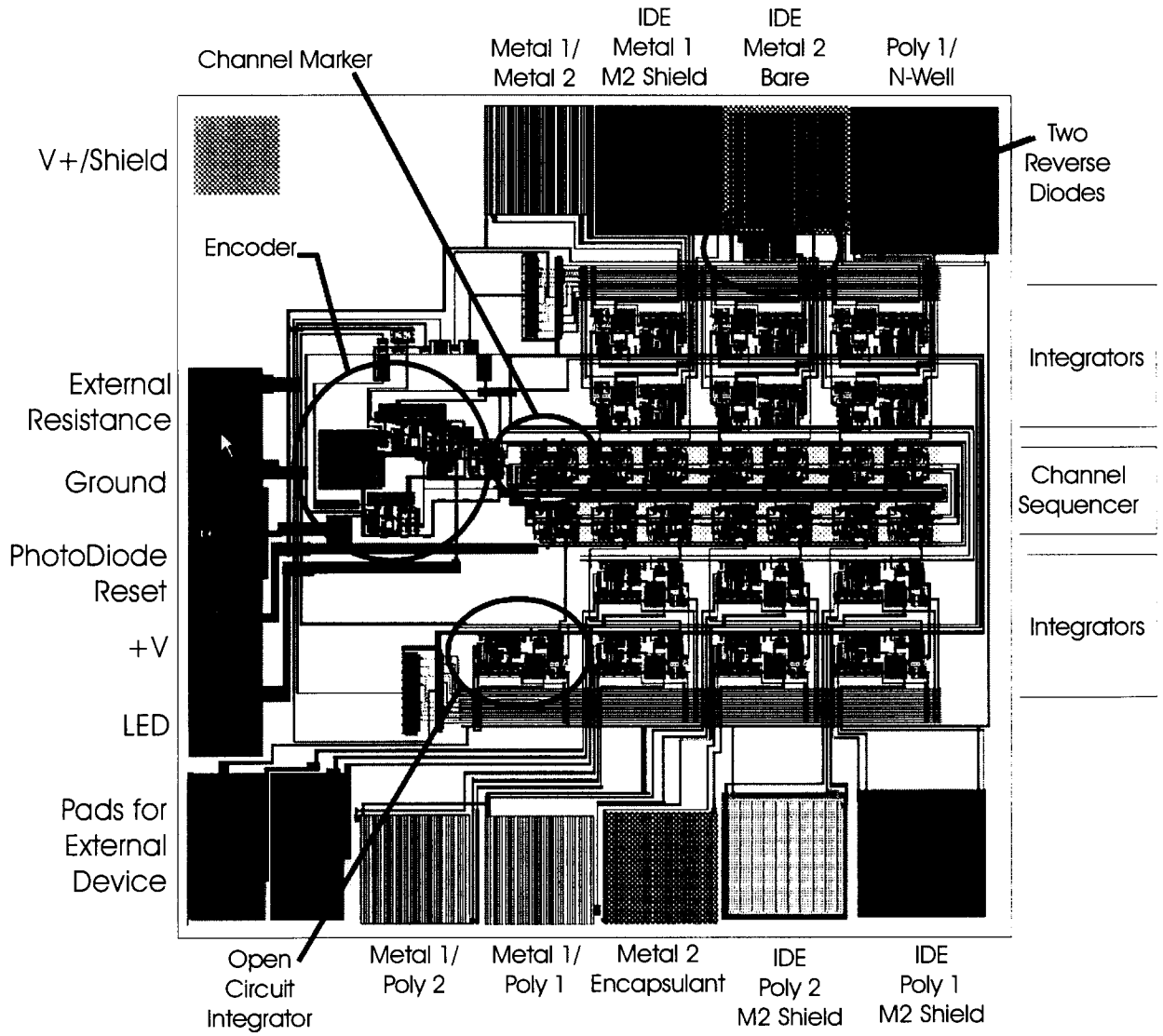

Figure 7: PassChip overview showing pad arrangement, test devices around periphery, channel sequencer and encoder in center corridor, and integrators between sequencer and test devices.

Pads for an external device were included to allow attachment of wire loops or some other external test device. They could also be connected with short wire loops to test bond pad leakage currents directly. The central corridor of the chip contains a loop of low power shift registers that continually cycle through the integrators to function as a channel sequencer. Double rows of integrators are located on either side of the shift registers. The test devices are connected to the integrators. The outputs of the integrators are bussed to the readout stage. The readout stage consists of switching to allow resetting of the readout capacitor high, then setting of the capacitor to the integrator output voltage using a p-channel source follower on the output of the

integrator being addressed. A 10nA current source pulls off the charge from the readout capacitor and then resets the readout capacitor. During the reset sequence, a pulse is generated for the LED transmitter.

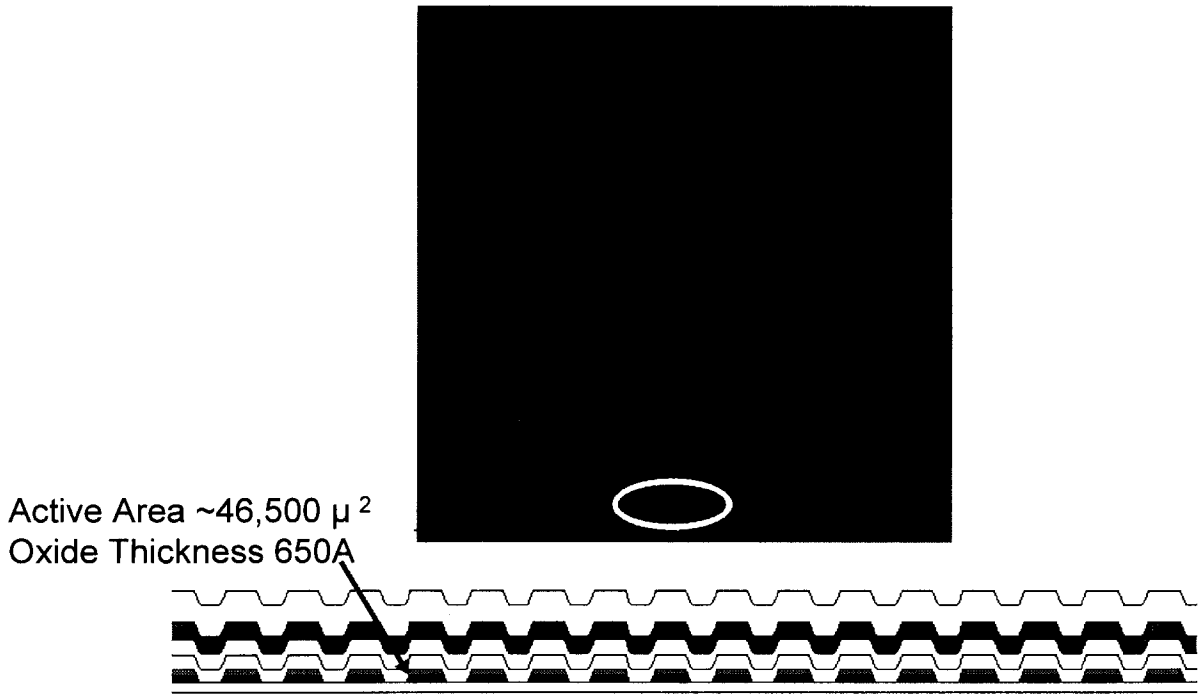

Figure 8: Example of vertical test structure shielded by Metal 2 (solid grey squiggle). Arrow points to one line of this multi-line structure with polysilicon 1 and polysilicon 2 separated by a thin silicon dioxide layer.

There were 14 channels included on this implementation. One channel was used for identifying Channel 1. Another channel was used to measure the open circuit leakage current of an integrator stage. Two channels were used to monitor the reverse biased leakage current of 3600μm^2 diodes. One of the diodes was shielded with Metal 2 and the other was not. Another channel was used for monitoring the external device bond pads. The remaining 9 devices were used for on-chip test structures. The on-chip test structures were of 2 varieties. One was an array of conductive fingers overlaying a second array of conductive fingers with the dielectric to be tested in between. These can be thought of as vertical testers and are designed to detect failure of the dielectric between two layers. An example of a vertical tester is shown in Figure 8. This structure consists of an array of lines of polysilicon on 2 layers separated by a thin silicon dioxide dielectric. The integrator will acquire electrons that flow from one polysilicon layer to the other through the thin dielectric. The active area is large and there are 2μm wide slots between every finger thereby ensuring that the device will be sensitive to water and ionic contamination. Vertical test devices included Metal 1 – Metal 2, Polysilicon 1 – N-Well, Metal 1 – Polysilicon 1, and Metal 1 to Polysilicon 2, and Metal 2 –Encapsulant. The Metal 2 – Encapsulant device was to measure the bulk resistivity of whatever encapsulant was used to protect the outer surface of the chip.

The second type of on-chip test device was the Interdigitated Electrode Array (IDEA). An example IDE testing the Metal 1 layer is shown in Figure 9. Because of the relatively small features and large test area, there are about 10^{-4}squares (□) for leakage current to flow. If the ultimate sensitivity of the measurement was be approximately $5x10^{-16}$amperes for a 5 volt bias, the effective surface resistivity that can be sensed would be approximately $10^{-20}\Omega/\square$ which should provide early indication of potential faults with MOS circuit protection in biological systems.

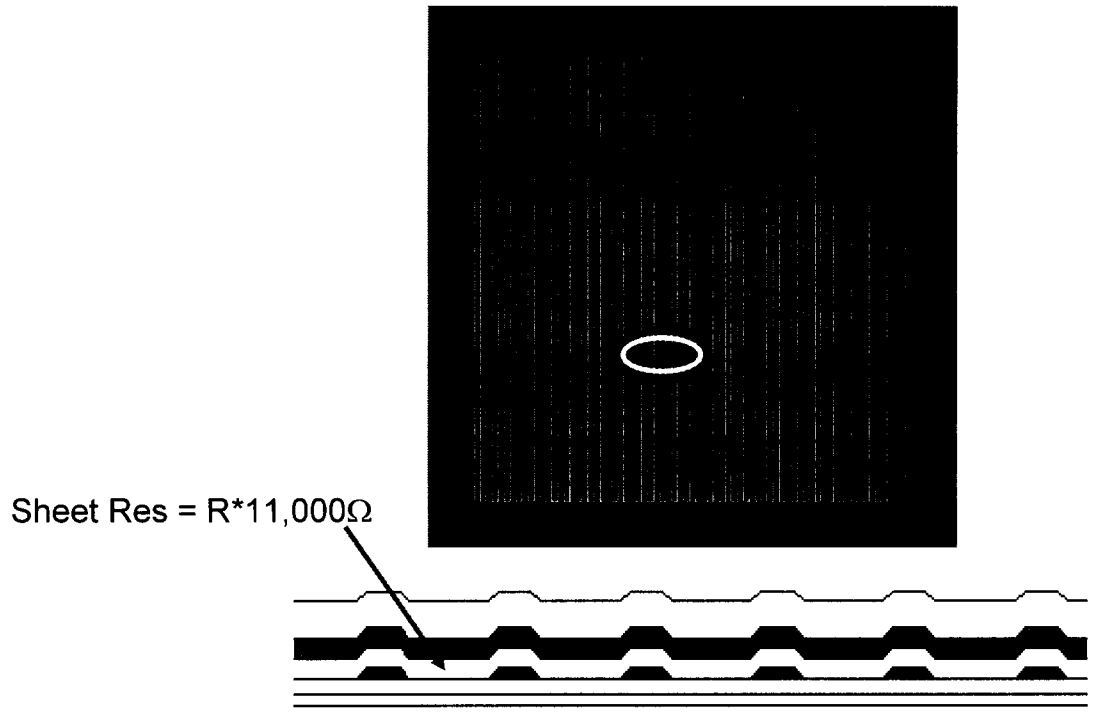

Figure 9: Interdigitated electrode array (IDEA) for MOSIS 2μm n-well process. IDEA is formed with Metal 1 while Metal 2 and the outer passivation layer provides additional protection.

Additional test circuits are being layed out for fabrication later this spring. It is anticipated that animal implants and *in-vitro* testing with these devices could be as soon as early summer, 1998.

SUMMARY OF PASSCHIP:

Vertical Grids Check Dielectric Conductivity
Interdigitated Electrode Arrays for Lateral Resistivity
MOS Threshold Monitors
Power and Bias Monitors
External Test Device Connections
Implantable in CNS with Transcutaneous Transmitter
Lithium TC Batteries Supply 4uA for >9years
Ultra-low power encode/mux/transmit circuit (3uA)